Srivatsa Vasudevan

Practical UVM

Step by Step with IEEE 1800.2

All code within this text was compiled and simulated with Synopsys® VCS P-2019.06 using Accellera UVM and the IEEE-1800.2 release.

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For more information, please contact:

Srivatsa Vasudevan
5567 Kimberly Street,
San Jose CA 95129
United States of America.

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This book is dedicated to:
The ONE by whose Grace,
A mute can speak eloquently,
A lame person can climb a mountain,
And for whom, nothing is impossible.
Our families and friends for supporting us
on this incredible journey.

Contents

Please Read! Important Note for the IEEE Edition

Dear Reader:

Thank you for purchasing this book, created to offer knowledge, theories, and practical examples to advance your knowledge and effective usage of SystemVerilog and UVM. This book is both current and rare; few publications support verification and other advancements related to the Universal Verification Methodology.

This book is the result of ”blood, sweat and tears” from many, including the author, graphic designers, editors and many in the UVM community on the inner workings of UVM. It has been prepared with considerable effort for your benefit with an effort spanning multiple years. I would greatly appreciate any feedback, suggestions, or comments; you have about this book - please send me your contribution to me via email, which is provided on the inside of the book cover. It shall be gratefully acknowledged.

The greatest profit to receive from the purchases of this book is donating all funds available after recovering the costs of creating this book and its distribution, to those in real need: *Those who suffer economic hardship with insufficient food for themselves and their children, and often without a place to call home or an opportunity to better themselves.*

Unauthorized copies, such as photocopied, DRM hacked or scanned, do not help us cover the costs, or offer the privilege and compassion enabling others to succeed as well. In many ways, your support of this book gives you an opportunity to help others as you advance your working knowledge of UVM for your own personal achievements.

I hope you will join me in this endeavor. Together, we can all make this world a better place.

Thank You
Srivatsa Vasudevan
Spring 2020

Changes Between the First Edition and the IEEE Edition

The order of chapters varies significantly between the First and IEEE editions. This reorganization was based on feedback from UVM trainers, who indicated that most new users would prefer to come up to speed on UVM and write stimulus quickly. Hopefully, this has been addressed in the UVM Quickstart - Part 1. Readers knowing UVM and wishing to obtain a more in-depth understanding may proceed to Parts II and III to gain in-depth knowledge. Advanced topics have been moved to Part III from Part V of the previous edition. Part IV provides complete practical examples, just like the previous edition. You will find some additional examples in this part as well that address topics in UVM 1800.2.

Readers have offered feedback related to editing and typographical errors in the first edition of this book. Considerable work has been put in to eliminate as many as possible. Many paragraphs were rewritten to clarify the intent and meaning. The book has also been reviewed by a technical writer.

If you work in a company, there is a good chance that you will be working with multiple UVM versions. When you are especially dealing with an SOC, where you inherit multiple environments, each at a different UVM version; things usually get a little interesting. Hence, this book attempts to serve all three different versions of the library UVM 1.1, UVM 1.2, and IEEE 1800.2. Version specific information (where available) is marked using the following icons:

This icon is for features new to UVM 1.2 from UVM 1.1 **ONLY**. If you see an issue between migration from UVM 1.1x to UVM 1.2, watch for this icon. If this feature has changed between the UVM 1.2 and IEEE 1800.2 versions, one of the other icons will also be present in the text adjacent to this icon.

Code/behavior that has changed between UVM 1.2 and IEEE 1800.2 is marked with this icon. Note that this icon is the same one used for the Accellera to IEEE standard implementation differences.

This icon is for features of UVM deprecated between 1.2 and IEEE 1800.2 **only**. It does not cover deprecation between UVM 1.2 and UVM 1.1x. See the migration guide in the previous chapter if you are attempting to migrate to the IEEE 1800.2 version from UVM 1.2.

This icon alerts you to features **new** in IEEE 1800.2 and not present in UVM 1.2. Please do not confuse this with features between UVM 1.2 and UVM 1.1x

Part 1:
This part is specifically geared to engineers wanting to pick up UVM quickly.

- Chapter 1 presents a UVM overview and helps Verilog users understand UVM testbench architecture and philosophy and make a transition to UVM.
- Chapter 2 introduces the UVM environment.
- Chapter 3 provides you with information on creating stimulus for your DUT in UVM quickly.

Part 2:

- Chapter 4 goes over changes to uvm_object and the associated core utilities. There are a number of changes in IEEE 1800.2, and you should review this chapter as UVM 1800.2 ***is not backward compatible*** with earlier versions.
- Chapter 5 goes over the additions to the UVM factory class to support abstract types and aliases. Additional examples are added for abstract classes and factory replacement.
- Chapter 8 on the UVM component hierarchy adds examples explaining the changes in the build_phase in UVM 1800.2, allowing you to speed things up.
- Chapter 6 goes over the changes to reporting in IEEE 1800.2. You may see additional failures in your regressions. Please review this chapter as additional changes may be required on your part in your scripts.
- Chapter 9 goes over callbacks and their behavior. Callbacks have been enhanced in IEEE 1800.2.
- The Register Abstraction layer has additional examples to illustrate IEEE capability. Chapter 20 discusses unlocking the register model.
- Chapter 13 on Phasing discusses changes with additional examples due to capabilities added in IEEE version.
- Chapter 14 discusses Advanced Stimulus Generation. The original chapter is partitioned from the earlier book to deal solely with advanced topics. Examples now use the UVM 1800.2 style.

Advanced Topics

- Chapter 15 provides examples of how to add event callbacks to an event, a new feature introduced in IEEE version.
- Chapter 19 has descriptions of the new capabilities in the common operations. Details on how to customize your environment using the capabilities of the IEEE version are included here.

Practical Applications:

- Chapter 21 uses a different comparison function in the scoreboard.
- Content on uvm_event, uvm_barrier has been relocated from Chapter 22 to Chapter 15.

Deprecated Core Utilities

Appendix A now describes the UVM 1.2 core utilities and behavior for compare/pack/print functions which have undergone enhancements in IEEE 1800.2. Some of the API described in this appendix has been deprecated in the IEEE version.